

Move Text Search Close

12 FEB 96 13:47:54 U.S. Patent & Trademark Office P0002

* The Help Desk staff at this number will handle all APS *
* related questions. *

* >>>>>>>>>> NEW SUNDAY HOURS !!! <<<<<<<<<<<<<<<<<

* The APS is available: *

* 6:30am - 9:00pm Monday through Friday *

* 7:30am - 5:00pm Saturday, Sunday, Holidays *

* APS is unavailable Thanksgiving Day, Christmas Day. *

* and New Year's Day. *

FILE 'USPAT' ENTERED AT 13:47:54 ON 12 FEB 96

* W E L C O M E T O T H E *

* U. S. P A T E N T T E X T F I L E *

=> act leadfram/a

'LEADFRAM/A' NOT FOUND

=> act leadframe/a

L1 (8464)SEA FILE=USPAT 174/52.1-52.4/CCLST OR 257/666,667,673,676,678

L2 (356)SEA FILE=USPAT (((CHIP (W) PACKAGE) OR (CHIP (W) CARRIER) OR

L3 (336)SEA FILE=USPAT (CHIP OR DIE) AND L2

L4 (296)SEA FILE=USPAT (LEAD#) AND L3

L5 (61)SEA FILE=USPAT (HOUSING#) AND L4

L6 235 SEA FILE=USPAT L4 NOT L5

=> s 14 and pn>19940601

438312 LEAD#

74834 CHIP

89867 DIE

9712 CHIP/AB

13279 PACKAGE/AB

99 CHIP (W) PACKAGE

9712 CHIP/AB

42594 CARRIER/AB

418 CHIP (W) CARRIER

42594 CARRIER/AB

13279 PACKAGE/AB

41 CARRIER (W) PACKAGE

24068 INTEGRATED/AB

145483 CIRCUIT/AB

252791 DEVICE/AB

938 INTEGRATED (W) CIRCUIT (W) DEVICE

2589 IC/AB

252791 DEVICE/AB

13:50:29 COPY AND CLEAR PAGE, PLEASE

INPUT:

<p>L-number to be added => 8</p> <p>Named Document Collection => 021296c</p> <p>Execute? (Y / N): y</p>	<p>P0005</p>
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507 29/854/CCLS
77 29/855/CCLS
1968 29/829,830,831,832,841,827,854,855/CCLS
((29/829 OR 29/830 OR 29/831 OR 29/832 OR 29/841 OR 29/827 0
R 29/854 OR 29/855)/CCLS)
814 437/209/CCLS
365 437/220/CCLS
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1126 437/209,220,224/CCLS
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191745 PD>19940601
(PD>19940601)
L8 62 L4 AND PD>19940601

=> save l8 rd0212c
'RD0212C' IS NOT A VALID SAVED NAME
ENTER NAME OR (END):rd0212c/a
ANSWER SET 'L8' HAS BEEN SAVED AS 'RD0212C/A'

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INPUT: _____

12 FEB 96 13:51:05 U.S. Patent & Trademark Office P0004
=> s 14 and pd>19940601
438312 LEAD#
74834 CHIP
89867 DIE
9712 CHIP/AB
13279 PACKAGE/AB
99 CHIP (W) PACKAGE
9712 CHIP/AB
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42594 CARRIER/AB
13279 PACKAGE/AB
41 CARRIER (W) PACKAGE
24068 INTEGRATED/AB
145483 CIRCUIT/AB
252791 DEVICE/AB
938 INTEGRATED (W) CIRCUIT (W) DEVICE
2589 IC/AB
252791 DEVICE/AB
125 IC (W) DEVICE
33950 SEMICONDUCTOR/AB
13279 PACKAGE/AB
232 SEMICONDUCTOR (W) PACKAGE
466 SC/AB
13279 PACKAGE/AB
0 SC (W) PACKAGE
24068 INTEGRATED/AB
13279 PACKAGE/AB
12 INTEGRATED (W) PACKAGE
24068 INTEGRATED/AB
252791 DEVICE/AB
63 INTEGRATED (W) DEVICE
3404 174/52.1-52.4/CCLST (4 TERMS)
(174/52.1+NEXT3/CCLST)
367 257/666/CCLS
62 257/667/CCLS
54 257/673/CCLS
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158 257/690/CCLS
200 257/692/CCLS
167 257/693/CCLS
171 257/704/CCLS
355 257/787/CCLS
18 257/789/CCLS
1705 257/666,667,673,676,678,684,690,692,693,704,787,789/CCLS
((257/666 OR 257/667 OR 257/673 OR 257/676 OR 257/678 OR 257
/684 OR 257/690 OR 257/692 OR 257/693 OR 257/704 OR 257/787
OR 257/789)/CCLS)
413 361/760/CCLS
220 361/772/CCLS
257 361/773/CCLS
290 361/816/CCLS
310 361/818/CCLS
151 361/829/CCLS
1531 361/760,772,773,816,818,829/CCLS
((361/760 OR 361/772 OR 361/773 OR 361/816 OR 361/818 OR 361
13:51:57 COPY AND CLEAR PAGE, PLEASE

INPUT:

Move NDC Addition Menu Execute

L-number to be added => 7

P0002

Named Document Collection => 021296a

Execute? (Y / N):

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* APS is unavailable Thanksgiving Day, Christmas Day,
* and New Year's Day.

FILE 'USPAT' ENTERED AT 08:19:59 ON 12 FEB 96

* W E L C O M E T O T H E *
* U . S . P A T E N T T E X T F I L E *

=> act leadframe

'LEADFRAME' MUST END IN '/Q', '/A', OR '/L'

ENTER NAME OF SAVED ITEM TO ACTIVATE OR (END):leadframe/a

L1 (8464)SEA FILE=USPAT 174/52.1-52.4/CCLST OR 257/666,667,673,676,678

L2 (356)SEA FILE=USPAT (((CHIP (W) PACKAGE) OR (CHIP (W) CARRIER) OR

L3 (336)SEA FILE=USPAT (CHIP OR DIE) AND L2

L4 (296)SEA FILE=USPAT (LEAD#) AND L3

L5 (61)SEA FILE=USPAT (HOUSING#) AND L4

L6 235 SEA FILE=USPAT L4 NOT L5

=> s 16 not pd > 19930930

268005 PD > 19930930

(PD>19930930)

L7 162 L6 NOT PD > 19930930

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INPUT:

12 FEB 96 08:58:27 U.S. Patent & Trademark Office P0002
* The Help Desk staff at this number will handle all APS *
* related questions. *
* * * * *
* >>>>>>>>>> NEW SUNDAY HOURS !!! <<<<<<<<<<<<<<< *
* The APS is available: *
* 6:30am - 9:00pm Monday through Friday *
* 7:30am - 5:00pm Saturday, Sunday, Holidays *
* APS is unavailable Thanksgiving Day, Christmas Day, *
* and New Year's Day. *
* * * * *
FILE 'USPAT' ENTERED AT 08:58:27 ON 12 FEB 96

* * * * *
* W E L C O M E T O T H E *
* U . S . P A T E N T T E X T F I L E *
* * * * *

=> act leadframe/a
L1 (8464)SEA FILE=USPAT 174/52.1-52.4/CCLST OR 257/666,667,673,676,678
L2 (356)SEA FILE=USPAT (((CHIP (W) PACKAGE) OR (CHIP (W) CARRIER) OR
L3 (336)SEA FILE=USPAT (CHIP OR DIE) AND L2
L4 (296)SEA FILE=USPAT (LEAD#) AND L3
L5 (61)SEA FILE=USPAT (HOUSING#) AND L4
L6 235 SEA FILE=USPAT L4 NOT L5

=> s l4 and transducer#
438312 LEAD#
74834 CHIP
89867 DIE
9712 CHIP/AB
13279 PACKAGE/AB
99 CHIP (W) PACKAGE
9712 CHIP/AB
42594 CARRIER/AB
418 CHIP (W) CARRIER
42594 CARRIER/AB
13279 PACKAGE/AB
41 CARRIER (W) PACKAGE
24068 INTEGRATED/AB
145483 CIRCUIT/AB
252791 DEVICE/AB
938 INTEGRATED (W) CIRCUIT (W) DEVICE
2589 IC/AB
252791 DEVICE/AB
125 IC (W) DEVICE
33950 SEMICONDUCTOR/AB
13279 PACKAGE/AB
09:00:09 COPY AND CLEAR PAGE, PLEASE

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Text Search

Close

12 FEB 96 09:00:27

U.S. Patent & Trademark Office

P0003

232 SEMICONDUCTOR (W) PACKAGE

466 SC/AB

13279 PACKAGE/AB

0 SC (W) PACKAGE

24068 INTEGRATED/AB

13279 PACKAGE/AB

12 INTEGRATED (W) PACKAGE

24068 INTEGRATED/AB

252791 DEVICE/AB

63 INTEGRATED (W) DEVICE

3404 174/52.1-52.4/CCLST (4 TERMS)

(174/52.1+NEXT3/CCLST)

367 257/666/CCLS

62 257/667/CCLS

54 257/673/CCLS

276 257/676/CCLS

241 257/678/CCLS

72 257/684/CCLS

158 257/690/CCLS

200 257/692/CCLS

167 257/693/CCLS

171 257/704/CCLS

355 257/787/CCLS

18 257/789/CCLS

1705 257/666,667,673,676,678,684,690,692,693,704,787,789/CCLS

((257/666 OR 257/667 OR 257/673 OR 257/676 OR 257/678 OR 257/684 OR 257/690 OR 257/692 OR 257/693 OR 257/704 OR 257/787 OR 257/789)/CCLS)

413 361/760/CCLS

220 361/772/CCLS

257 361/773/CCLS

290 361/816/CCLS

310 361/818/CCLS

151 361/829/CCLS

1531 361/760,772,773,816,818,829/CCLS

((361/760 OR 361/772 OR 361/773 OR 361/816 OR 361/818 OR 361/829)/CCLS)

231 29/829/CCLS

366 29/830/CCLS

121 29/831/CCLS

382 29/832/CCLS

190 29/841/CCLS

458 29/827/CCLS

307 29/854/CCLS

77 29/855/CCLS

1968 29/829,830,831,832,841,827,854,855/CCLS

((29/829 OR 29/830 OR 29/831 OR 29/832 OR 29/841 OR 29/827 OR 29/854 OR 29/855)/CCLS)

814 437/209/CCLS

365 437/220/CCLS

77 437/224/CCLS

1126 437/209,220,224/CCLS

((437/209 OR 437/220 OR 437/224)/CCLS)

74701-TRANSDUCER#

L7

0 L4 AND TRANSDUCER#

=> s l4 and ((thermal (w) coefficient (w) expansion) or (tce))

438312 LEAD#

09:02:46 COPY AND CLEAR PAGE, PLEASE

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Move Text Search Close

12 FEB 96 09:03:09 U.S. Patent & Trademark Office P0005

121 29/831/CCLS
 382 29/832/CCLS
 190 29/841/CCLS
 458 29/827/CCLS
 307 29/854/CCLS
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 1968 29/829,830,831,832,841,827,854,855/CCLS
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 R 29/854 OR 29/855)/CCLS)
 814 437/209/CCLS
 365 437/220/CCLS
 77 437/224/CCLS
 1126 437/209,220,224/CCLS
 ((437/209 OR 437/220 OR 437/224)/CCLS)
 249270 THERMAL
 114400 COEFFICIENT
 155778 EXPANSION
 37 THERMAL (W) COEFFICIENT (W) EXPANSION
~~921 TCE~~
 L8 6 L4 AND ((THERMAL (W) COEFFICIENT (W) EXPANSION) OR (TCE))

=> d ti 1-6

US PAT NO: 5,471,027 [IMAGE AVAILABLE] L8: 1 of 6
 TITLE: Method for forming **chip** carrier with a single protective
 encapsulant

US PAT NO: 5,455,446 [IMAGE AVAILABLE] L8: 2 of 6
 TITLE: Leaded semiconductor package having temperature controlled
lead length

US PAT NO: 5,367,124 [IMAGE AVAILABLE] L8: 3 of 6
 TITLE: Compliant **lead** for surface mounting a **chip** package to a
 substrate

US PAT NO: 5,158,912 [IMAGE AVAILABLE] L8: 4 of 6
 TITLE: Integral heatsink semiconductor package

US PAT NO: 4,890,194 [IMAGE AVAILABLE] L8: 5 of 6
 TITLE: A **chip** carrier and mounting structure connected to the
chip carrier

US PAT NO: 4,682,270 [IMAGE AVAILABLE] L8: 6 of 6
 TITLE: Integrated circuit **chip** carrier

=> s l4 and (downset (w) lead)

438312 LEAD#
 74834 CHIP
 89867 DIE
 9712 CHIP/AB
 13279 PACKAGE/AB
 99 CHIP (W) PACKAGE
 9712 CHIP/AB
 42594 CARRIER/AB
 418 CHIP (W) CARRIER
 42594 CARRIER/AB
 13279 PACKAGE/AB
 41 CARRIER (W) PACKAGE

09:05:38 COPY AND CLEAR PAGE, PLEASE

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Move Text Search Close

12 FEB 96 09:06:00 U.S. Patent & Trademark Office P0007
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1126 437/209,220,224/CCLS
((437/209 OR 437/220 OR 437/224)/CCLS)
50 DOWNSET
305923 LEAD
1 DOWNSET (W) LEAD
L9 0 L4 AND (DOWNSET (W) LEAD)

=> s 14 and downset
438312 LEAD#
74834 CHIP
89867 DIE
9712 CHIP/AB
13279 PACKAGE/AB
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42594 CARRIER/AB
418 CHIP (W) CARRIER
42594 CARRIER/AB
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41 CARRIER (W) PACKAGE
24068 INTEGRATED/AB
145483 CIRCUIT/AB
252791 DEVICE/AB
938 INTEGRATED (W) CIRCUIT (W) DEVICE
2589 IC/AB
252791 DEVICE/AB
125 IC (W) DEVICE
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13279 PACKAGE/AB
232 SEMICONDUCTOR (W) PACKAGE
466 SC/AB
13279 PACKAGE/AB
0 SC (W) PACKAGE
24068 INTEGRATED/AB
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12 INTEGRATED (W) PACKAGE
24068 INTEGRATED/AB
252791 DEVICE/AB
63 INTEGRATED (W) DEVICE
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(174/52.1+NEXT3/CCLST)
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1705 257/666,667,673,676,678,684,690,692,693,704,787,789/CCLS
((257/666 OR 257/667 OR 257/673 OR 257/676 OR 257/678 OR 257
/684 OR 257/690 OR 257/692 OR 257/693 OR 257/704 OR 257/787
OR 257/789)/CCLS)

09:09:02 COPY AND CLEAR PAGE, PLEASE

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12 FEB 96 09:09:20 U.S. Patent & Trademark Office P0008
413 361/760/CCLS
220 361/772/CCLS
257 361/773/CCLS
290 361/816/CCLS
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231 29/829/CCLS
366 29/830/CCLS
121 29/831/CCLS
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1968 29/829,830,831,832,841,827,854,855/CCLS
((29/829 OR 29/830 OR 29/831 OR 29/832 OR 29/841 OR 29/827 OR 29/854 OR 29/855)/CCLS)
814 437/209/CCLS
365 437/220/CCLS
77 437/224/CCLS
1126 437/209,220,224/CCLS
((437/209 OR 437/220 OR 437/224)/CCLS)
50 DOWNSET
L10 4 L4 AND DOWNSET

=> d ti 1-4

US PAT NO: 5,457,341 [IMAGE AVAILABLE] L10: 1 of 4
TITLE: Integrated circuit device and manufacturing method using photoresist **lead** covering

US PAT NO: 5,429,992 [IMAGE AVAILABLE] L10: 2 of 4
TITLE: **Lead** frame structure for IC devices with strengthened encapsulation adhesion

US PAT NO: 5,422,313 [IMAGE AVAILABLE] L10: 3 of 4
TITLE: Integrated circuit device and manufacturing method using photoresist **lead** covering

US PAT NO: 4,842,662 [IMAGE AVAILABLE] L10: 4 of 4
TITLE: Process for bonding integrated circuit components

=> s l4 and (silicone (w) gel)
438312 LEAD#

74834 CHIP
89867 DIE
9712 CHIP/AB
13279 PACKAGE/AB
99 CHIP (W) PACKAGE
9712 CHIP/AB
42594 CARRIER/AB
418 CHIP (W) CARRIER
42594 CARRIER/AB
13279 PACKAGE/AB
41 CARRIER (W) PACKAGE

09:11:06 COPY AND CLEAR PAGE, PLEASE

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12 FEB 96 09:35:33 U.S. Patent & Trademark Office P0010
77 437/224/CCLS
1126 437/209,220,224/CCLS
((437/209 OR 437/220 OR 437/224)/CCLS)
74713 SILICONE
124937 GEL
~~714 SILICONE (W) GEL~~
L11 4 L4 AND (SILICONE (W) GEL)

=> d ti 4

US PAT NO: 4,663,650 [IMAGE AVAILABLE] L11: 4 of 4
TITLE: Packaged integrated circuit **chip**

=> d t 1-3

'T' IS NOT A VALID FORMAT FOR FILE 'USPAT'
ENTER DISPLAY FORMAT (CIT):d ti 1-3
'D' IS NOT A VALID FORMAT FOR FILE 'USPAT'
'1-3' IS NOT A VALID FORMAT FOR FILE 'USPAT'
YOU HAVE RECEIVED THIS ERROR MESSAGE 2 CONSECUTIVE TIMES

The following are valid formats:

PNO ----- Patent Number
PAT ----- Patent Number, Issue Date, and Current Original
 Reference Classification
CIT ----- Patent Number, Issue Date, Title,
 First Inventor Name, and Current Classifications
LEG ----- Patent Number, Issue Date, Title, Inventor, Assignee,
 Appl. Number, Filing Date, Art Unit, Primary Examiner,
 Legal Rep., Rule 47 Indicator, Attorney Reg. Number
REF ----- Classification and Reference Information
DATE ----- PCT Information and all dates from Front Page
PCT ----- Alias for the DATE Format
BIB ----- Alias for the LEG Format
FRO ----- Front Page Information, Art Unit, and Current
 Classifications
ALL ----- Entire Patent and Key words assigned
FUL ----- Alias for the ALL Format
SPC ----- Alias for the ALL Format
CLS ----- Patent Number and Current Classification
PN ----- Patent Number
OCC ----- Occurrence Count
AB ----- Abstract
FD ----- Application Filing Date
AD ----- Application Filing Date
AN ----- Application Number with Series Code
ART ----- Art Unit
AS ----- Assignee Information
ATT ----- Attorney, Agent or Firm
BSUM ----- Summary
CCLS ----- Current Classification
CLMS ----- Claims Information
D371 ----- PCT 371 Date
DD ----- Disclaimer Date
DETD ----- Detail Description
DRWD ----- Drawing Description
E102 ----- PCT 102(e) Date
ECL ----- Exemplary Claim Number
FREF ----- Foreign Patent References Cited
09:36:11 COPY AND CLEAR PAGE, PLEASE

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12 FEB 96 09:36:24 U.S. Patent & Trademark Office P0011
FS ----- Field of Search U.S. Classifications and IPCs
GI ----- Government Interest Text Data
ICLS ----- Issue Classification
IN ----- Inventor Information
IPC ----- International Classification
OREF ----- Other Publication References Cited
PARN ----- Parent Case Text Data
PD ----- Issue Date
PPDR ----- Number of Drawing Sheets
PPSP ----- Number of Specification Pages
PRIR ----- Foreign Application Priority
PTAN ----- PCT Number
PTFD ----- PCT Filing Date
PTPD ----- PCT Publication Date
PTPN ----- PCT Publication Number
REI ----- Reissue Data
REL ----- Related Application Data
TERM ----- Term Of Patent
TI ----- Title
UREF ----- U. S. Patent References Cited
XA ----- Assistant Examiner
XP ----- Primary Examiner
KEY ----- Keywords Identified for Patent
IF YOU REQUIRE FURTHER HELP, PLEASE CONTACT YOUR LOCAL HELP DESK
ENTER DISPLAY FORMAT (CIT):end

=> d ti 1-3

US PAT NO: 5,394,009 [IMAGE AVAILABLE] L11: 1 of 4
TITLE: Tab semiconductor package with cushioned land grid array outer
lead bumps

US PAT NO: 5,386,342 [IMAGE AVAILABLE] L11: 2 of 4
TITLE: Rigid backplane formed from a moisture resistant insulative
material used to protect a semiconductor device

US PAT NO: 5,072,283 [IMAGE AVAILABLE] L11: 3 of 4
TITLE: Pre-formed chip carrier cavity package

=> d l4 and polymer

'L4' HAS NO ANSWERS

L1 (8464)SEA FILE=USPAT 174/52.1-52.4/CCLST OR 257/666,667,673,676,678
684,690,692,693,704,787,789/CCLS OR 361/760,772,773,816,818,
829/CCLS OR 29/829,830,831,832,841,827,854,855/CCLS OR 437/20
9,220,224/CCLS

L2 (356)SEA FILE=USPAT (((CHIP (W) PACKAGE) OR (CHIP (W) CARRIER) OR
(CARRIER (W) PACKAGE) OR (INTEGRATED (W) CIRCUIT (W) DEVICE)
OR (IC (W) DEVICE) OR (SEMICONDUCTOR (W) PACKAGE) OR (SC (W)
PACKAGE) OR (INTEGRATED (W) PACKAGE) OR (INTEGRATED (W) DEVI
CE))/AB) AND L1

L3 (336)SEA FILE=USPAT (CHIP OR DIE) AND L2

L4 (296)SEA FILE=USPAT (LEAD#) AND L3

=> s l4 and polymer#

438312 LEAD#

74834 CHIP

89867 DIE

9712 CHIP/AB

09:38:27 COPY AND CLEAR PAGE, PLEASE

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12 FEB 96 09:40:11 U.S. Patent & Trademark Office P0013
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 307 29/854/CCLS
 77 29/855/CCLS
 1968 29/829,830,831,832,841,827,854,855/CCLS
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 R 29/854 OR 29/855)/CCLS)
 814 437/209/CCLS
 365 437/220/CCLS
 77 437/224/CCLS
 1126 437/209,220,224/CCLS
 ((437/209 OR 437/220 OR 437/224)/CCLS)

L12 218894-POLYMER#
32 L4 AND POLYMER#

=> d 1

1. 5,483,098, Jan. 9, 1996, Drop-in heat sink package with window frame
 flag; Bennett A. Joiner, Jr., 257/676, 719, 796 [IMAGE AVAILABLE]

=> d 2-34

32 ANSWERS ARE AVAILABLE. SPECIFIED ANSWER NUMBER EXCEEDS ANSWER SET SIZE
 ENTER ANSWER NUMBER OR RANGE (1):2-32

2. 5,471,027, Nov. 28, 1995, Method for forming **chip** carrier with a single
 protective encapsulant; Anson J. Call, et al., 219/85.13; 29/841, 855;
 437/211, 902 [IMAGE AVAILABLE]

3. 5,457,341, Oct. 10, 1995, Integrated circuit device and manufacturing
 method using photoresist **lead** covering; David W. West, 257/666, 667,
 668 [IMAGE AVAILABLE]

4. 5,457,071, Oct. 10, 1995, Stackable vertical thin package/plastic molded
lead-on-**chip** memory cube; Edward J. Dombroski, 437/217, 209, 214, 219,
 220 [IMAGE AVAILABLE]

5. 5,455,745, Oct. 3, 1995, Coated bonding wires in high **lead** count
 packages; Peter M. Weiler, et al., 361/813; 174/52.4; 257/690; 361/807,
 808 [IMAGE AVAILABLE]

6. 5,422,313, Jun. 6, 1995, Integrated circuit device and manufacturing
 method using photoresist **lead** covering; David W. West, 437/217, 214, 219,
 220 [IMAGE AVAILABLE]

7. 5,386,342, Jan. 31, 1995, Rigid backplane formed from a moisture
 resistant insulative material used to protect a semiconductor device; Michael
 Rostoker, 361/749; 174/52.2, 52.3, 252, 254; 257/668, 790; 361/707, 750,
 807, 809; 439/67, 77, 485 [IMAGE AVAILABLE]

8. 5,358,906, Oct. 25, 1994, Method of making integrated circuit package
 containing inner **leads** with knurled surfaces; Hee G. Lee, 437/217;
 257/666; 437/220, 977 [IMAGE AVAILABLE]

9. 5,319,242, Jun. 7, 1994, Semiconductor package having an exposed **die**
 surface; Francis J. Carney, et al., 257/680, 673, 675, 692, 702, 735,
 737, 774, 782 [IMAGE AVAILABLE]

10. 5,302,778, Apr. 12, 1994, Semiconductor insulation for optical devices;
 Martin A. Maurinus, 174/52.4; 257/432 [IMAGE AVAILABLE]

09:41:27 COPY AND CLEAR PAGE, PLEASE

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Move Text Search Close

- 12 FEB 96 09:41:41 U.S. Patent & Trademark Office P0014
11. 5,270,261, Dec. 14, 1993, Three dimensional multichip package methods of fabrication; Claude L. Bertin, et al., 437/209; 148/DIG.135; 437/208, 228, 974 [IMAGE AVAILABLE]
12. 5,237,203, Aug. 17, 1993, Multilayer overlay interconnect for high-density packaging of circuit elements; Laurence I. Massaron, 257/688, 690, 719, 727, 759, 773, 785 [IMAGE AVAILABLE]
13. 5,202,754, Apr. 13, 1993, Three-dimensional multichip packages and methods of fabrication; Claude L. Bertin, et al., 257/684, 723, 725, 777 [IMAGE AVAILABLE]
14. 5,157,588, Oct. 20, 1992, Semiconductor package and manufacture thereof; Gu S. Kim, et al., 361/736; 174/52.4; 361/717, 784 [IMAGE AVAILABLE]
15. 5,147,210, Sep. 15, 1992, Polymer film interconnect; Timothy P. Patterson, et al., 439/91; 29/830, 832; 156/273.9 [IMAGE AVAILABLE]
16. 5,139,973, Aug. 18, 1992, Method for making a semiconductor package with the distance between a lead frame die pad and heat spreader determined by the thickness of an intermediary insulating sheet; Bela G. Nagy, et al., 437/211, 214, 220, 902 [IMAGE AVAILABLE]
17. 5,085,362, Feb. 4, 1992, Gravity-held alignment member for manufacture of a leadless chip carrier; Jack Art, et al., 228/49.1; 29/760, 827, 840; 228/122.1 [IMAGE AVAILABLE]
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27. 4,766,670, Aug. 30, 1988, Full panel electronic packaging structure and method of making same; Charles E. Gazdik, et al., 29/830, 593, 840; 361/751; 437/205 [IMAGE AVAILABLE]
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30. 4,618,739, Oct. 21, 1986, Plastic chip carrier package; Paul R. Theobald, 174/52.4; 437/1, 215; 439/68 [IMAGE AVAILABLE]
31. 4,552,267, Nov. 12, 1985, Ceramic semiconductor package chip prevention structure and method; Francis W. Layher, 257/724; 174/52.2, 52.4; 206/593, 713, 718; 257/678; 437/218, 219 [IMAGE AVAILABLE]
32. 4,355,719, Oct. 26, 1982, Mechanical shock and impact resistant ceramic semiconductor package and method of making the same; Sally K. Hinds, et al., 206/713; 174/52.2; 206/593, 718; 257/678; 437/215, 218 [IMAGE AVAILABLE]

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29. 4,682,270, Jul. 21, 1987, Integrated circuit **chip** carrier; Graham K. Whitehead, et al., 361/764; **174/52.4**; 257/702, 706; 361/709, 768 [IMAGE AVAILABLE]

30. 4,618,739, Oct. 21, 1986, Plastic **chip** carrier package; Paul R. Theobald, **174/52.4**; 437/1, 215; 439/68 [IMAGE AVAILABLE]

31. 4,552,267, Nov. 12, 1985, Ceramic semiconductor package **chip** prevention structure and method; Francis W. Layher, 257/724; **174/52.2**, **52.4**; 206/593, 713, 718; **257/678**; 437/218, 219 [IMAGE AVAILABLE]

32. 4,355,719, Oct. 26, 1982, Mechanical shock and impact resistant ceramic semiconductor package and method of making the same; Sally K. Hinds, et al., 206/713; **174/52.2**; 206/593, 718; **257/678**; 437/215, 218 [IMAGE AVAILABLE]

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L13 6 (L8 OR L10 OR L11) AND L12

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US PAT NO: 5,471,027 [IMAGE AVAILABLE] L13: 1 of 6
TITLE: Method for forming **chip** carrier with a single protective encapsulant

US PAT NO: 5,457,341 [IMAGE AVAILABLE] L13: 2 of 6
TITLE: Integrated circuit device and manufacturing method using photoresist **lead** covering

US PAT NO: 5,422,313 [IMAGE AVAILABLE] L13: 3 of 6
TITLE: Integrated circuit device and manufacturing method using photoresist **lead** covering

US PAT NO: 5,386,342 [IMAGE AVAILABLE] L13: 4 of 6
TITLE: Rigid backplane formed from a moisture resistant insulative material used to protect a semiconductor device

US PAT NO: 4,890,194 [IMAGE AVAILABLE] L13: 5 of 6
TITLE: A **chip** carrier and mounting structure connected to the **chip** carrier

US PAT NO: 4,682,270 [IMAGE AVAILABLE] L13: 6 of 6
TITLE: Integrated circuit **chip** carrier

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